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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 05/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/059,644	Applicant(s) PAN, PAI-HUNG	
	Examiner Michael M Trinh	Art Unit 2822	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *41 and 43-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *41 and 43-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

*** This office action is in response to Applicant's Amendment filed on March 04, 2002. Claims 41,43-53 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102/103

1. Claims 41,45,46,50 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurimoto (5,306,655).

Kurimoto teaches a method (at Figs 13a-13h; col 13, line 21 through col 16) for forming a conductive gate of a metal oxide transistor comprising the steps of: forming a gate str3ucture having a polysilicon gate electrode 5f formed on a gate oxide dielectric layer 2 formed on a semiconductor substrate (figs 13a; col 13, lines 30+); forming barrier sidewall nitride spacers 10 over sidewalls of the gate electrode and joining the dielectric oxide layer 2 by anisotropically etching a silicon nitride layer 10 (figs 13C-13D); and then oxidizing the substrate to channel oxidants through the gate dielectric layer 2 and underneath the spacers joined therewith and which is outwardly exposed laterally proximate the sidewall spacers, wherein only a portion of the gate electrode 5f, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 2 is oxidized (Fig 13f), while preventing oxidation of the upper parts of side faces of the gate electrode 5f by the action of the barrier insulating nitride spacers 10 (col 13, lines 59-68), wherein as recited at column 18, lines 4-21, a third insulating film consisting of material which is not readily permeable to oxygen is formed over the gate electrode, wherein an intervening oxide layer is not formed between the gate electrode and the third insulating film.

2. Claims 41,45,46,50 are rejected under 35 U.S.C. 102(b) as being anticipated by, or in the alternative under 35 USC 103 (a) as unpatentable over Verhaar (5,015,598) with Hiroki et al (5,512,771) as an evidence also.

Verhaar teaches a method (at Figs 1-5; col 4, line 30 through col 5) for forming a conductive gate of a metal oxide transistor comprising the steps of: forming a gate structure having a polysilicon gate electrode 12 formed on a gate oxide dielectric layer 11 formed on a semiconductor substrate 10 (col 4); forming barrier sidewall nitride spacers 20a laterally adjacent

the sidewalls of the gate electrode 12 and joining the dielectric oxide layer 10 by anisotropically etching a silicon nitride layer 20 (col 4, lines 45-49; col 5, lines 10-52); and then oxidizing the substrate to channel oxidants through the gate dielectric layer 10 (col 5, lines 47-52) and underneath the spacers joined therewith and which is outwardly exposed laterally proximate the sidewall spacers, wherein only a portion of the gate electrode 12, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 10 is oxidized (Fig 5), while preventing oxidation of the upper parts of side faces of the gate electrode 12 by the action of the barrier insulating nitride spacers 10. Since Verhaar discloses forming the silicon nitride spacers 20a having a thickness between 15 and 50 nm and preferably close to 30 nm (col 4, lines 63-68) adjacent to the gate electrode 12; and since oxidizing at 900°C for a duration of 15 to 30 minutes in oxygen to form a silicon oxide layer 24 (fig 5) having a thickness of the order of 10 to 15 nm (100 to 150 Angstroms), only a portion only a portion of the gate electrode 12, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 10 is inherently oxidized and creating a "smiling gate" (can be seen by enlarging the gate electrode), wherein as shown from Figures 4 to 6 of Verhaar, after forming spacers 20a and prior to forming source and drain regions 22a,23a (Fig 6), exposing the substrate to oxidizing conditions to create a "smiling gate" (Figs 4-6). It is the fact that the present specification discloses (at page 7, lines 14-19) that only portion of the gate electrode is oxidized in a time period for growing "an oxide layer over a separate semiconductor substrate to a thickness of a round 80 Angstroms". Herein, since Verhaar grows a silicon oxide layer 24 having a thicker thickness of 100 to 150 Angstroms, only a portion of the gate electrode, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 10, is inherently oxidized ("smiling gate"). Consequently, the burden shifted to applicant to demonstrate and prove that this apparent inherence does not in fact exist, In re King, 801 F.2d 1324, 1327, 231 USPQ 136, 138-139 (Fed. Cir. 1986).

Regarding 102 rejection, Hiroki et al (5,512,771) is evidently cited to show that the oxide layer 6' formed under the silicon nitride spacer 7 allows oxidizing substance to transmit therethrough to oxidize a portion of the gate electrode to form a "smiling gate" (col 12, lines 10-21; figs 6A-6B).

Regarding 103 rejection, as in the alternative: Hiroki et al (5,512,771) teach to form a "smiling gate" by oxidizing a portion of the gate electrode, laterally adjacent the sidewall spacers

and at the interface with the gate dielectric layer, wherein the oxide layer 6' underlying the silicon nitride spacer 7 allows oxidizing substance to transmit therethrough to oxidize a portion of the gate electrode to form a "smiling gate" (col 12, lines 10-21; figs 6A-6B), wherein as shown from Figure 6A to Figure 6D of Hiroki, after forming spacers and prior to forming source and drain regions 3 (Fig 6D; col 12), exposing the substrate to oxidizing conditions to create a "smiling gate" (Figs 6B-6C). Thus, it would have been obvious to ordinary skill in the art to create a "smiling gate" as taught by Hiroki et al by oxidizing a portion of the gate electrode of Verhaar, wherein a portion of the oxide layer 11 underlying the spacers 20a as shown in figure 11 allows oxidizing substance to transmit therethrough to oxidize a portion of the gate electrode to form a "smiling gate". This is because of the desirability to have smaller gate-to-drain capacitance and thus to improve the speed of the circuit operation (col 8, lines 45-67; fig 2).

Claim Rejections - 35 USC § 103

3. Claims 43,47 are rejected under 35 U.S.C. § 103(a) as being unpatentable over either Verhaar/Hiroki et al OR Kurimoto (5,306,655), in view of Pintchovski et al (5,126,283).

Verhaar/Hiroki already teaches a method for forming a conductive gate of a metal oxide transistor as applied above to claims 41,45,46,50. Kurimoto teaches a method for forming a semiconductor device as applied above to claims 45,46.

Either Verhaar/ Hiroki or Kurimoto lack to form a gate electrode having a polysilicon, a conductive reaction barrier layer, and an overlying metal (re claims 43,47).

However, Pintchovski et al teach (at figs 3a-3c; col 5, line 60 through col 6, line 45) to alternatively form a gate electrode having a polysilicon layer 38, a conductive reaction barrier layer 40, and an overlying metal 42.

The subject matter would have been obvious to one of ordinary skill in the art at the time the invention was made to form a multi-layered transistor gate electrode as taught by Pintchovski et al because of the desirability to fabricate high speed devices due to high conductivity of the gate electrode, wherein the conductive reaction barrier layer also acts as a diffusion barrier.

4. Claims 44,48,49,51,52,53 are rejected under 35 U.S.C. § 103(a) as being unpatentable over either Verhaar/Hiroki et al (5015598 & 5512771) OR Kurimoto (5,306,655) in view of

Pintchovski et al (5,126,283), as applied to claims 41,43,45-47,50 above, and further of Brigham et al (5,714,413) and Kumagai et al (5,430,313).

Verhaar/Hiroki or Kurimoto already teaches to form single sidewall barrier spacers over sidewalls of the gate (similarly to a first embodiment of the present invention as shown in figure 3 having a single sidewall barrier spacers 34).

The further main difference between the references applied above and the instant claim(s) is as follows: instead of using single sidewall spacers (first embodiment, fig 3 of present application), the present application, in a second embodiment (fig 5) and a third embodiment (fig 7), alternatively teaches to use double sidewall spacers by etching first and second material layers.

However, Brigham et al teach (at figs 2b-2c,3c; col 6, line 60 through col 7, line 6; cols 4-6) to form double sidewall spacers by depositing a second material layer on a first material layer and anisotropically etching the first and second layers to form double sidewall spacers, wherein Brigham expressly teaches "three or more layers of dielectric...are implemented to form a multi-layered spacer structures" (col 6, lines 1-6), and wherein silicon nitride is disclosed. Kumagai et al teach (at figs 4B-4D; col 3, line 65 through col 4, line 15) to form single sidewall nitride spacers 16 on sidewalls of a gate 14, and alternatively, forming double sidewall nitride spacers including first sidewall nitride spacers 16 and second sidewall nitride spacers 30 by anisotropically etching a deposited first material barrier layer and then anisotropically etching a second deposited material barrier layer (figs 7A-7D; col 5, line 45 through col 6).

The subject matter would have been obvious to one of ordinary skill in the art at the time the invention was made to alternatively form single sidewall nitride spacers or double sidewall spacers on the sidewalls of the gate as combinatively taught by Brigham, Kumagai, and Verhaar. This is because of the desirability to substitute and alternatively use the single sidewall nitride spacers or the double sidewall spacers as a barrier mask during oxidation to form an oxide film. This is also because of the desirability to employ the double sidewall spacers as a mask during implantation to form source and drain regions at a predetermined distance from the gate electrode.

Response to Arguments

5. Applicant's arguments filed March 04, 2002 have been fully considered but they are not persuasive, and are moot in view of new ground(s) of rejection.

6. Regarding Kurimoto references under 35 USC 102 rejection: Applicant deleted "...and prior to forming source/drain region..." by this amendment filed March 04, 2002. Accordingly, the Kurimoto (5,306,655) reference as applied in previous office action is now outstanding and anticipated subject matter of claims 41,45,46,50.

7. <u>Regarding Verhaar with Hiroki et al:</u>

** Regarding 35 USC 102 rejection using Verhaar, with Hiroki as evidence:

Applicant mainly remarked (at 3/4/02 remark, page 13-14, begin from first full paragraph) that " ...Verhaar is void of any teaching of oxidizing gate material..." , "Verhaar explicitly teaches that oxidation is limited to parts of the device.... Verhaar...does not provide any teaching, disclosure, suggestion or motivation to oxidize gate material...".

In response, this is noted and found unconvincing. Applicant appears to mis-interpretation the teachings of Verhaar. First, arguendo that "Verhaar is void of any teaching of oxidizing gate material" or "Verhaar explicitly teaches that oxidation is limited to parts of the device". Under 35 USC 102 rejection, Verhaar still anticipated the claimed invention regardless whether explicitly oxidizing the gate material or avoiding and teaching away from oxidizing the gate material. In other words, Verhaar already recognized and disclosed oxidation of the gate material even taught away from that oxidation.

Second, in the other hand, as applied in the office action, Verhaar discloses forming the silicon nitride spacers 20a having a thickness between 15 and 50 nm and preferably close to 30 nm (col 4, lines 63-68) adjacent to the gate electrode 12, in which oxidizing at 900°C for a duration of 15 to 30 minutes in oxygen to form a silicon oxide layer 24 (fig 5) having a thickness of the order of 10 to 15 nm (100 to 150 Angstroms), only a portion only a portion of the gate electrode 12, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 10 is inherently oxidized and creating a "smiling gate" (can be seen by enlarging the gate electrode). As shown from Figures 4 to 6 of Verhaar, after forming spacers 20a and prior to forming source and drain regions 22a,23a (Fig 6), exposing the substrate to oxidizing conditions to create a "smiling gate" (Figs 4-6). It is the fact that the present specification discloses (at

page 7, lines 14-19) that only portion of the gate electrode is oxidized in a time period for growing "an oxide layer over a separate semiconductor substrate to a thickness of a round 80 Angstroms". Herein, since Verhaar grows a silicon oxide layer 24 having a thicker thickness of 100 to 150 Angstroms, only a portion of the gate electrode, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 10, is inherently oxidized ("smiling gate"). Consequently, the burden shifted to applicant to demonstrate and prove that this apparent inherence does not in fact exist, In re King, 801 F.2d 1324, 1327, 231 USPQ 136, 138-139 (Fed. Cir. 1986). Furthermore, it is the fact that Hiroki et al (5,512,771) is evidently cited to show that the oxide layer 6' formed under the silicon nitride spacer 7 allows oxidizing substance to transmit therethrough to oxidize a portion of the gate electrode to form a "smiling gate" (col 12, lines 10-21; figs 6A-6B).

Applicant is further mistaken by asserting (at remark page 15) that "...Verhaar explicitly teaches controlling these process variables in such a manner to limit oxidation ...to show exactly and only this in Figs 5-10". Nowhere in the specification of Verhaar is expressly stated to form the device showing "exactly and only this in Figs 5-10" and controlling the processing parameters to limit what is and what is not oxidized.

** Regarding 35 USC 103 rejection using Verhaar with Hiroki :

Applicant mainly remark (at remark page 15, last paragraph) that "Hiroki et al teach formation of an oxide layer 6 adjacent a gate structure 5b. In contrast, Applicant recites 'forming sidewall spacers comprising nitride on the gate electrode's sidewalls, the sidewall joining with the gate dielectric layer...".

In response, this is noted and found unconvincing. Under 35 USC 103 rejection, the primary reference of Verhaar clearly teach that limitations.

Applicant further remark (at remark page 16) that Hiroki et al do not teach, disclose, suggest or motivate the invention...".

In response, this is noted and found unconvincing. Hiroki et al (5,512,771) prima facie teach, suggest, or motivate to form a "smiling gate" by oxidizing a portion of the gate electrode, laterally adjacent the sidewall spacers and at the interface with the gate dielectric layer, wherein the oxide layer 6' formed under the silicon nitride spacer 7 allows oxidizing substance to

transmit therethrough to oxidize a portion of the gate electrode to form a "smiling gate" (col 12, lines 10-21; figs 6A-6B). Hiroki shows the "oxide layer 6' formed under silicon nitride spacer 7 allowing the oxidizing substance to transmit therethrough to oxide a portion of the gate electrode". Therefore, it would have been obvious to ordinary skill in the art to create a "smiling gate" as taught by Hiroki et al by oxidizing a portion of the gate electrode of Verhaar. This is because of the desirability to have smaller gate-to-drain capacitance and thus to improve the speed of the circuit operation (col 8, lines 45-67; fig 2).

Applicant's previously remarks about "modification of Verhaar would render it unsatisfactory for its intended purpose" are noted and found unconvincing. In combination, by oxidizing to form a "smiling gate", *both* purposes including regenerating of the polluted silicon oxide under the nitride spacer *and* obtaining a device having smaller gate-to-drain capacitance and improved speed of the circuit operation can be obtained at about the same time in a single oxidation step.

** Applicant remarks (at remark page 16, last paragraphs) about Pintchovski are noted and found unconvincing. Pintchovski et al merely cited to show (at figs 3a-3c; col 5, line 60 through col 6, line 45) that it would have been obvious to form a gate structure having a polysilicon layer 38, a conductive reaction barrier layer 40, and an overlying metal 42 because of the desirability to fabricate high speed devices due to high conductivity of the gate electrode, wherein the conductive reaction barrier layer also acts as a diffusion barrier.

** Applicant remarks (at remark pages 16-17) about Brigham and Kumagai et al are noted and found unconvincing. Brigham and Kumagai clearly teach to form double sidewall spacers by etching first and second material layers. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to alternatively form single sidewall nitride spacers or double sidewall spacers on the sidewalls of the gate as combinatively taught by Brigham, Kumagai, and Verhaar. This is because of the desirability to substitute and alternatively use the single sidewall nitride spacers or the double sidewall spacers as a barrier mask during oxidation to form an oxide film. This is also because of the desirability to employ the double sidewall spacers as a mask during implantation to form source and drain regions at a predetermined distance from the gate electrode.

*** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Whitehead Jr Carl can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs

Michael Trinh
Primary Examiner